SMART SOLUTIONS TO DRIVE THE FUTURE

Technology Roadmap of SINGULUS Solar

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Hamburg, September 6th 2011

SINGULUS TECHNOLOGIES AG

Introduction

- Industrial production of PV modules has reached a very cost competitive phase. Nevertheless, grid parity is not yet reached.
  Further improvement of production cost and cell efficiency is required to fully establish solar electricity as one of the future's most significant energy sources.

- SINGULUS TECHNOLOGIES is well prepared to actively drive the required further technological development based on the decisive core processes and products in both wet chemical and vacuum deposition technologies.

- Additional equipment and processes are in development and are ready to be transferred into industrial mass production in both most promising cell technologies - crystalline silicon and in CIGS thin film.

- Improved or new technologies can be evolutionary transferred into system business. Disruptive technology improvements are in preparation.

Roadmap Crystalline Si-Cells: Basic Approach

Today

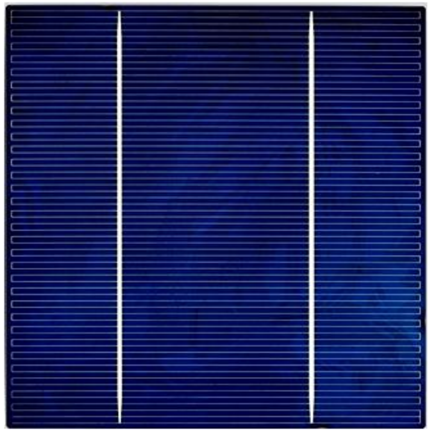
- Machine in production
- Standard processes developed
- High-efficiency processes in development
- Co-operations with several interested institutes and lead customers for new cell concepts in progress

Tomorrow

- Application of high efficiency cell processes on existing equipment
- Introduction of new equipment for advanced cell concepts
- Integration of high efficiency processes into system business

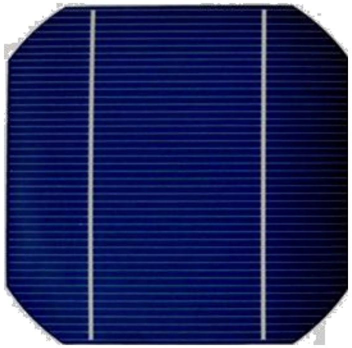
Present Conversion Efficiencies

Multi-crystalline Si-Cell



Cell properties mc-Si cell *			
η [%]	V_{oc} [mV]	I_{sc} [mA/cm^2]	FF [%]
17.0	626	34.8	78.1

Mono-crystalline Si-Cell



Cell properties mono Si cell **			
η [%]	V_{oc} [mV]	I_{sc} [mA/cm^2]	FF [%]
18.6	628	37.7	78.7

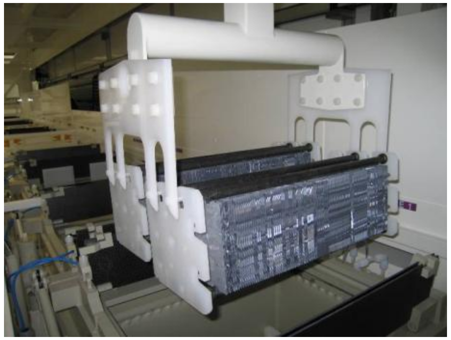
***   2011, 156x156 mm2 screen printed cell, industrial production**
**** 2011, 156x156 mm2 screen printed cell, industrial production**

Wet and Vacuum Processes -
The Decisive Steps for High Efficiency Cell Production

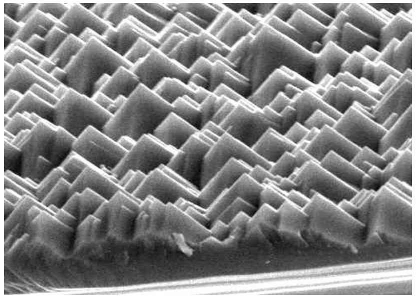
Standard	ASPIRe	EWT	RISE EWT	IBC	i PERC	LFC PERC
Texture	Structuring: Holes (Laser)	Structuring: Holes (Laser)	Pass rear + masking for Emitterdiffusion: SiO_2 (Wet Oxidation)	Texture: Aniso	Texture: Iso (Wet/Plasma)	Pass rear: SiO_2 (Thermal Oxidation)
POCl	Texture: Iso	Etching: LDE along with SDR	Etching: Oxdide front	POCl	POCl front	Etching: Oxdide front
PSG	POCl	Texture	Texture: Aniso	Structuring: Emitter removal + rear surface	PSG	Texture: Aniso
ARC + Pass: SiN_x front	Structuring: Rear emitter removal + rear surface	Selective Emitter: Diffusion barier with open channels {1}	Structuring: ablation rear & hole drilling (Laser)	PSG	ARC + Pass: SiN_x front	POCl
Metall1: Ag front (Screen Print)	PSG	POCl	Etching: LDE	ARC + Pass: SiN_x front	Pass: SiO_x rear	PSG
Metall2: Al + Ag rear (Screnn Print)	ARC+ Pass: SiN_x front	PSG	POCl	Pass: SiO_x rear	Mirror: SiN_x rear	ARC + Pass: Oxidation SiO_2 front
Firing: Furnace Co	Pass: SiN_x rear	ARC + Pass: SiN_x front	PSG	Mirror: SiN_x rear	Structuring: Opening pass/mirror rear (Laser)	Structuring: Opening front grid (Laser)
Isolation: Laser	Metall1: Ag front + rear + holes (Screen Print)	Pass: SiN_x rear	ARC + Pass: double SiN_x front	Firing: Pass *Furnace?*	Metall1: Al rear (Evaporation)	Metall1: Ti/Pd/Ag front (Evaporation)
	Metall2: Al rear (Screen Print)	Metall1: Al p-contact = open channels {1} (Screen Print)	Oxidation (Tunneloxid for emitter-contact): SiO_2 (Thermal)	Metall1: Al (Lithographic + Evaporation)	Metall2: Ag front (Screen Print)	Metall2: Al rear (Evaporation)
	Firing: Furnace Co	Metall2: Al n-contact + connecting holes (Screen Print)	Metall: Al rear (Evaporation)	Metall1: Mask lift off	Firing: Furnace Co	Firing: rear locally (Laser)
		Firing: Furnace Co	SiO_2: Etchbarrier rear (Evaporation)	Firing: Al *Furnace?*		Metall3: Ag front (Plating)
			Etching/Isolation: Al flanks	Metall2: Ti/Pd/Ag (Lithographic + Evaporation)		
			Firing: Base (Laser)	Metall2: Mask lift off		
				Forming gas anneal		

Design-To-Cost - Advanced Alkaline Texturing

- **New development of a cost saving anisotropic texturing process for well established platform SILEX**
  (> 120 installed systems in the field)

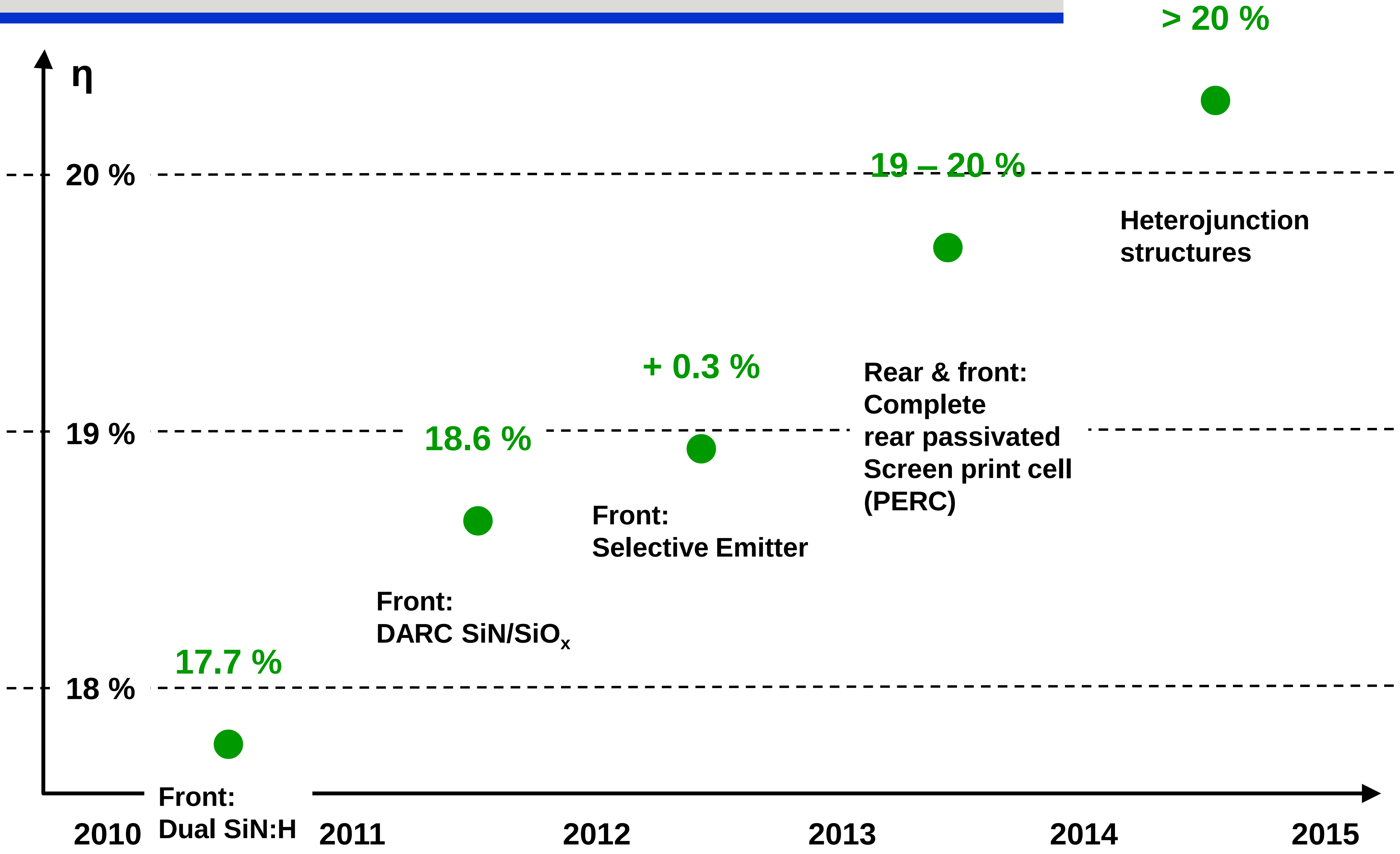


- **Advantages of new texturing agent vs. standard IPA texturing**
  - \+ Flammability risks eliminated
  - \+ Improved process stability, simple application
  - \+ Extended bath lifetime (min. 30 runs) > less waste disposal
  - \+ Smaller, more uniform pyramid size compared to other solutions
  - \+ Shorter etching time
  - \+ Improved environmental impact (less evaporation loss, less waste water)
  - \+ Process works on Standard SILEX ALTEX (upgrade package required)



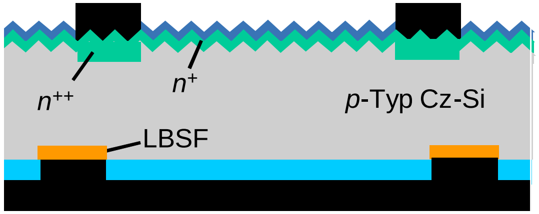
- **Process applicable for all standard and high efficiency cell concepts based on monocrystalline wafer material**

Technology and Efficiency Roadmap



Technology and Efficiency Roadmap

- **Selective Emitter**
  - industrial partnership if required for System Business
  - efficiency + 0,3 %, time frame 12 months f



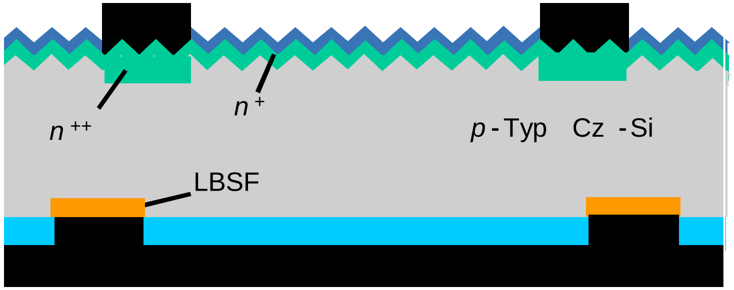
- **Rear Passivated Screen Print Cell**
  - Institutional R&D project for 3 years regarding passivation layers
  - feasibility for passivation layer proven on SINGULAR in two variations
  - industrial implementation of passivation layer possible from today
  - complete inline-solution (System Business) can be provided in approximately 12 - 18 months
  - target efficiency 19 – 20 % on mono c-Si cells
  - evolutionary technology development

- **Heterojunction Structures**
  - R&D project for 3 years has started together with SERIS
  - if feasible: transfer into industrial production in 2014
  - disruptive technology development, however well suited for SINGULAR platform

Concept - PERC

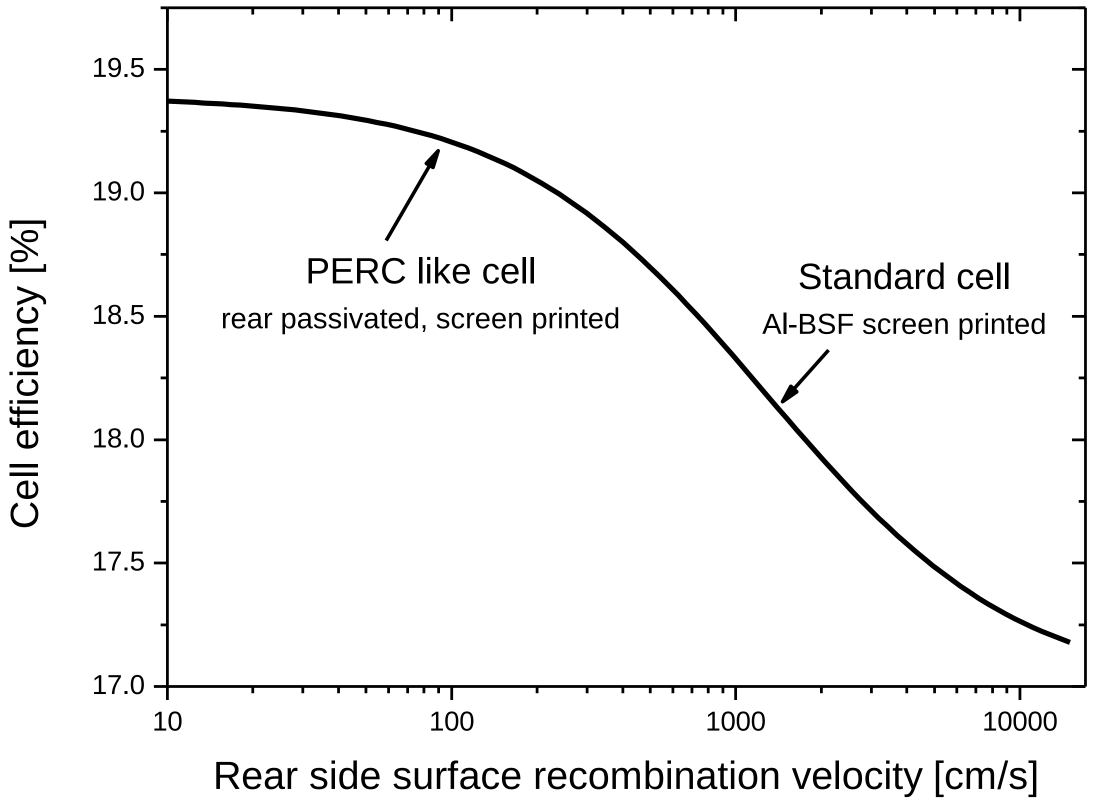
PERC - Passivated emitter and rear cell

"The PERC cell is often suggested as a relatively low cost way for making silicon cells above 20% efficiency." , **Martin A. Green, 2001**



SDE / Front TEX | **Back polish** → **P-Diff** → **PSG** | Pre- treat ↓ **Rear Pass** ↑ **Front Pass & ARC** → **Print /FFF/ Test & Sort**

PERC – Surface Recombination Velocity (SRV)



Surface Recombination Velocity (SRV)

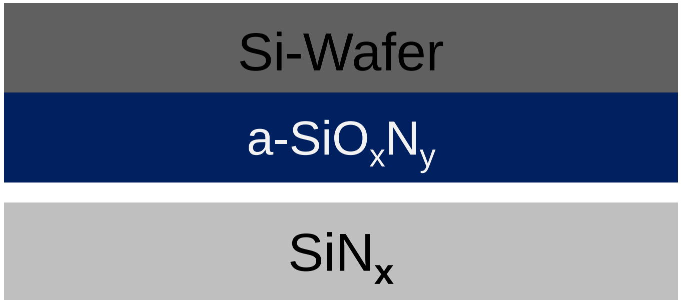
A measure of the rate of recombination between electrons and holes at the surface of a semiconductor.

→ The lower the SRV, the higher the cell efficiency can be !

SINGULAR – Rear passivation

SINGULUS is following two ways to achieve rear side passivation

Solution 1: a-SiO_xN_y / SIN

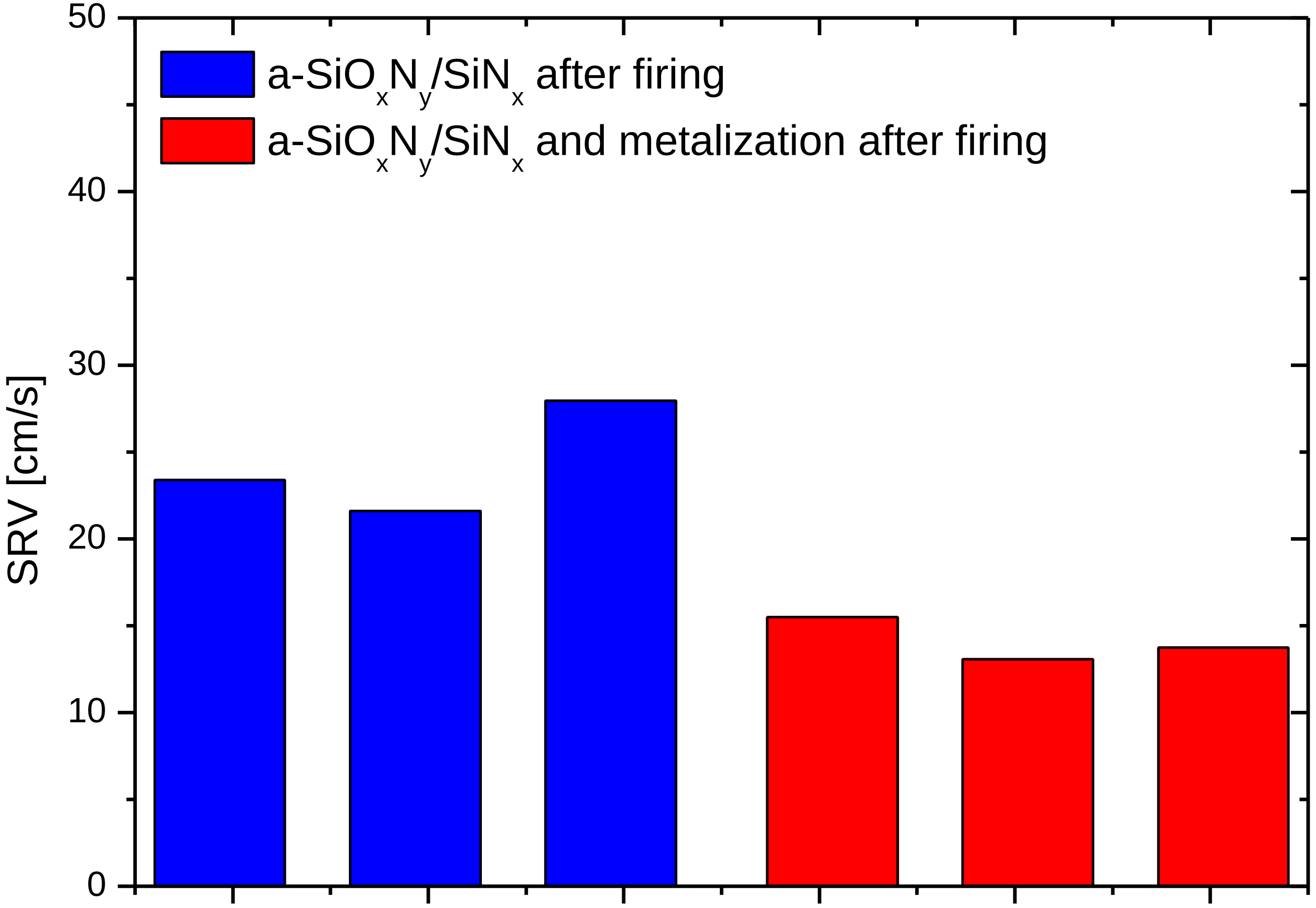


Solution 2: Al_2O_3 / SIN

Feasibility studies have shown that both layer stacks can be applied with the SINGULAR deposition technology. Both solutions show very good surface recombination velocities.

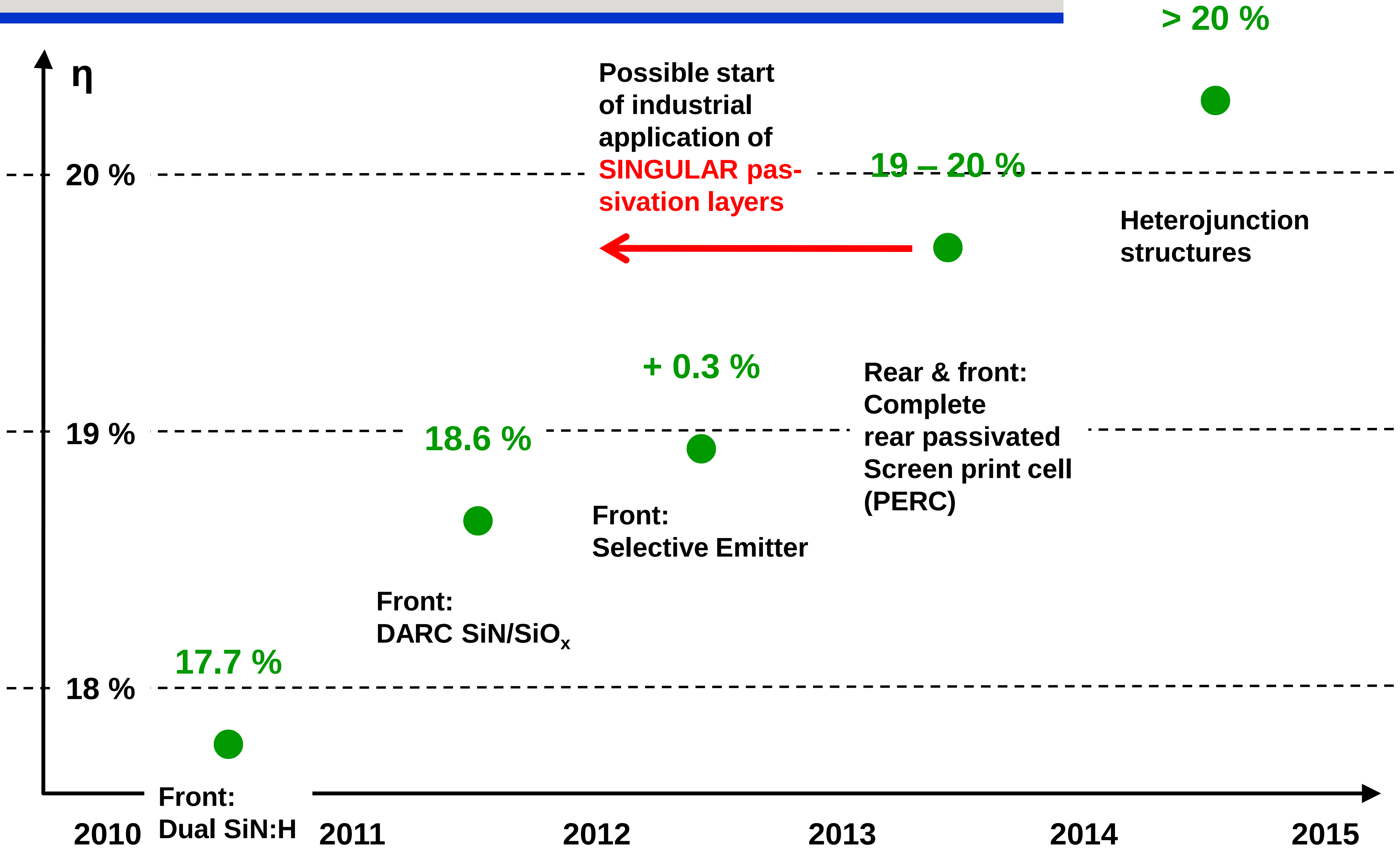
At least one of the two solutions will be further followed for a transfer into industrial production with help of the mass production tool SINGULAR. Discussions with industrial partners are ongoing.

Results - Solution 1 – The silicon way



* Data achieved in cooperation with T. Dullweber, ISFH

Summary Roadmap c-Si



17.7 %

Front:
Dual SiN:H

18.6 %

Front:
DARC SiN/SiO$_x$

+ 0.3 %

Front:
Selective Emitter

19 – 20 %

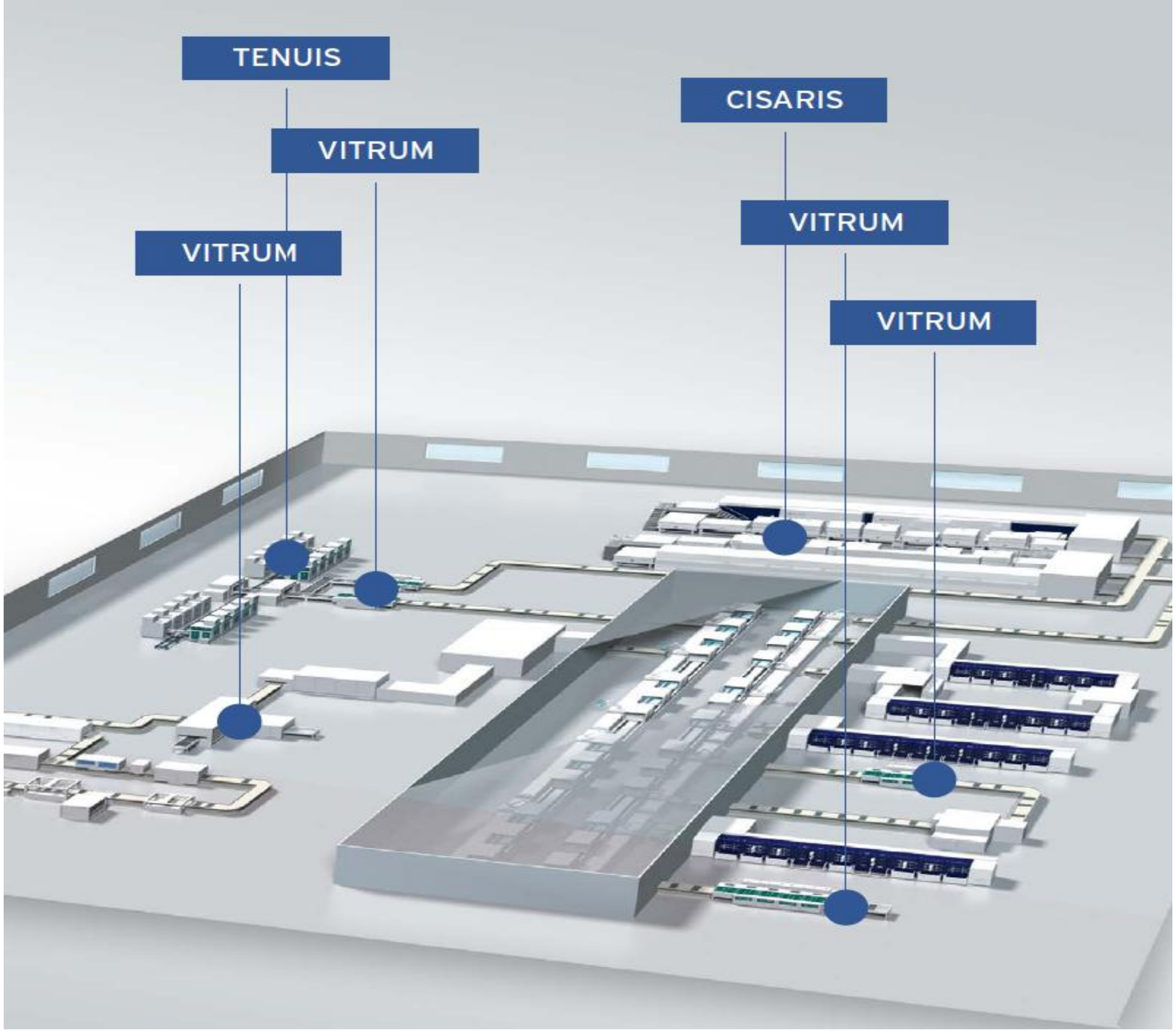
Rear & front:
Complete
rear passivated
Screen print cell
(PERC)

Possible start
of industrial
application of
SINGULAR passivation layers

> 20 %

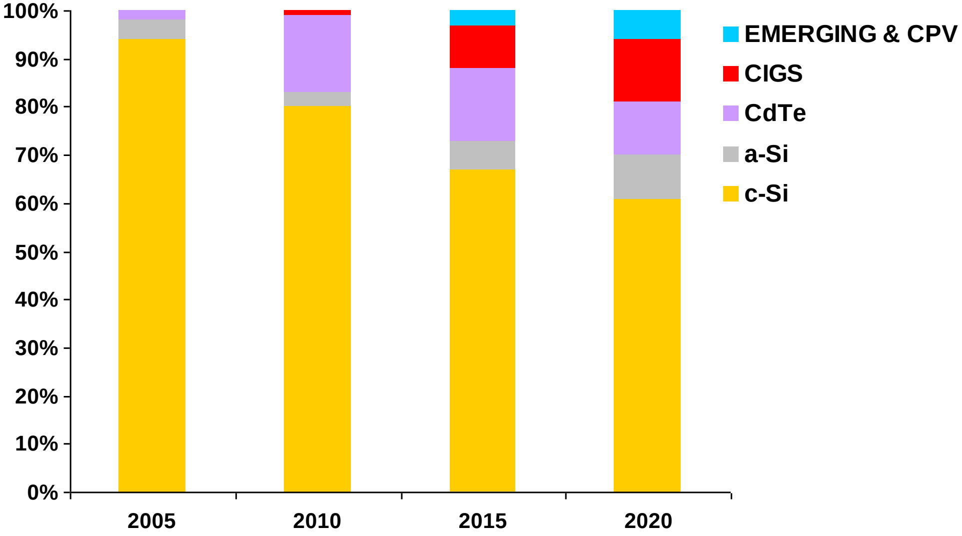
Heterojunction
structures

SINGULUS Thin Film - Focus on CIGS



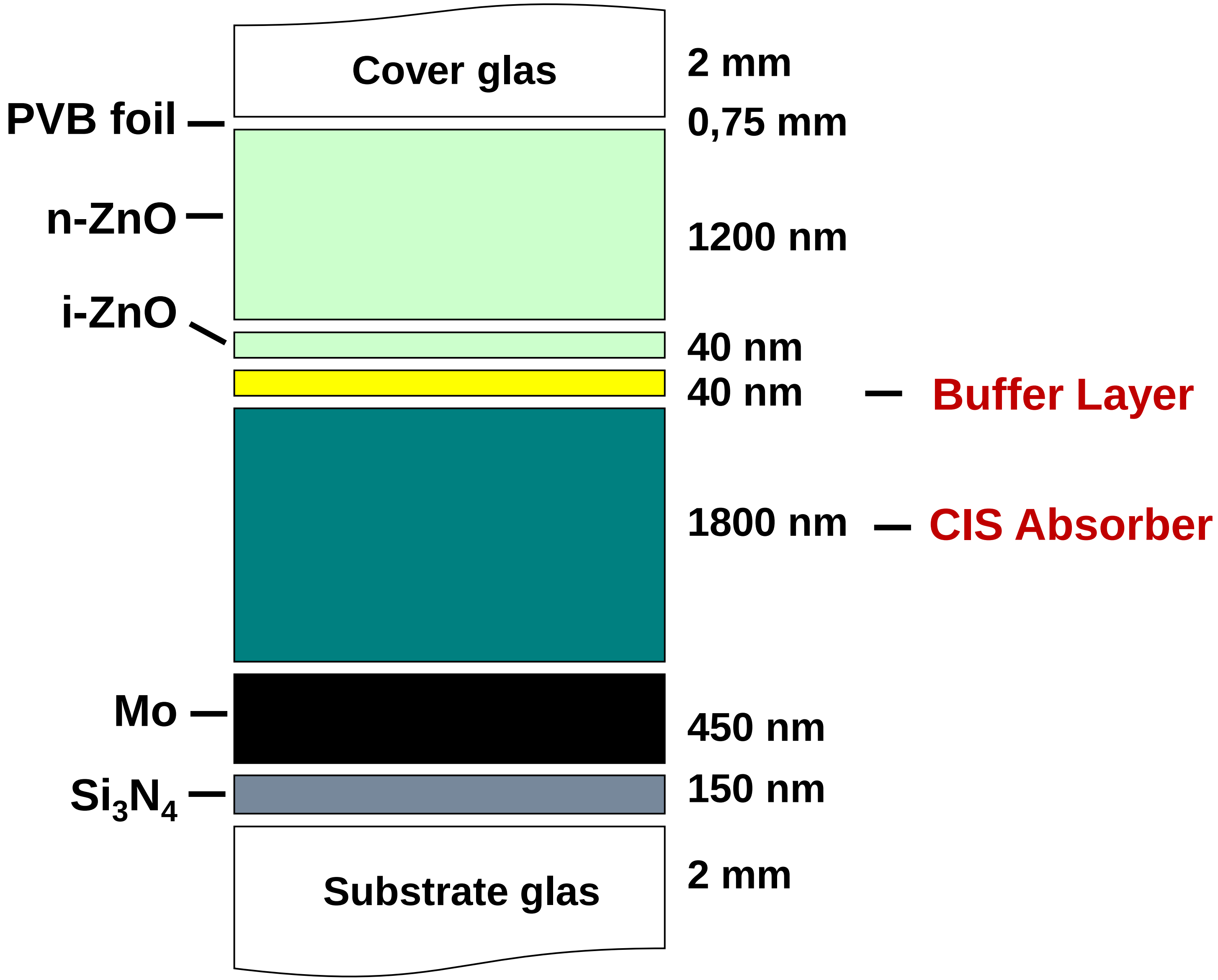
Thin Film - Why CIGS?

- High efficiencies (more than 20% in the lab, more than 13% in production)
- High technological threshold, but well established and reliable technology
- Low manufacturing costs
- Limited number of competitors
- High innovation potential
- Aesthetic module design, branding of proprietary module technology



Source: Historical data (until 2009) based on Navigant Consulting. Estimations based on EPIA analysis.

Typical Layout of a CIGS Module



Layer	Thickness	
Cover glas	**2 mm**	
PVB foil	**0,75 mm**	
n-ZnO	**1200 nm**	
i-ZnO	**40 nm**	
	40 nm	**Buffer Layer**
	1800 nm	**CIS Absorber**
Mo	**450 nm**	
Si_3N_4	**150 nm**	
Substrate glas	**2 mm**	

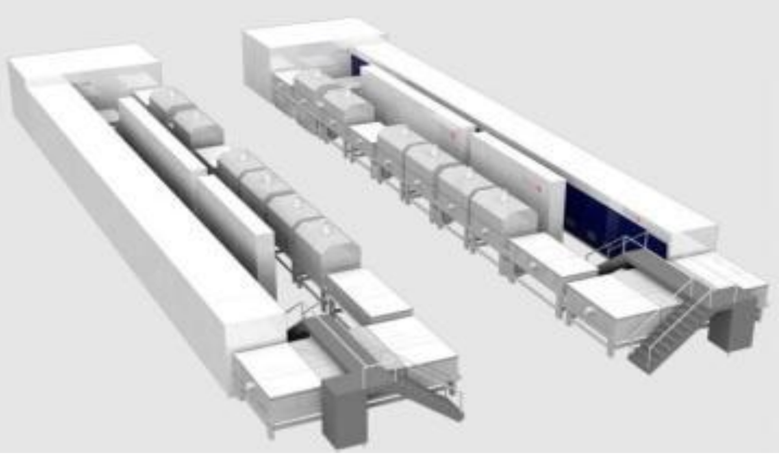
SINGULUS products

TENUIS / IMPEDIO and ILGAR

CISARIS
(for certain applications)

plus: **VITRUM**
for all cleaning and etching steps

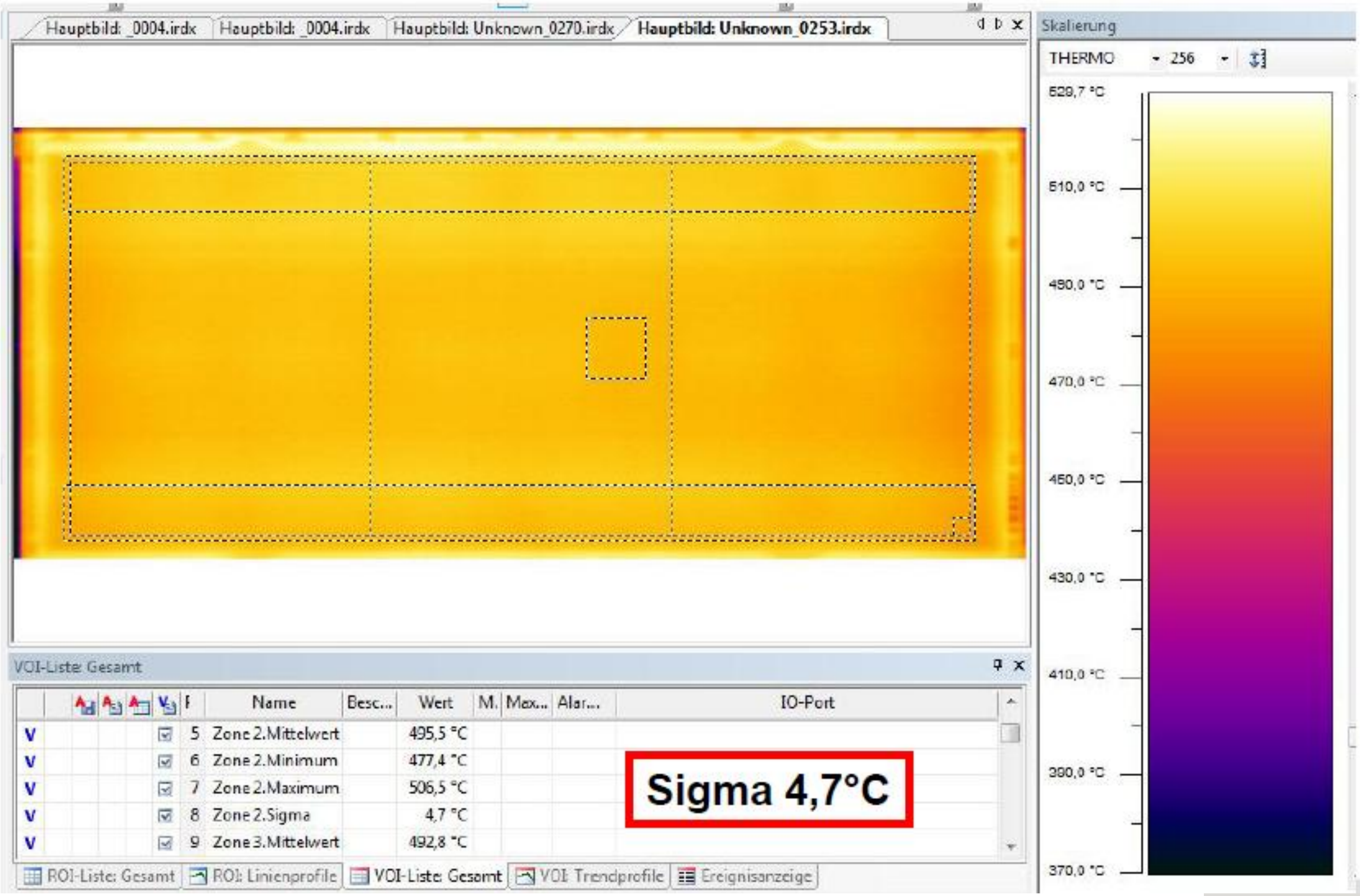
CISARIS Inline Diffusion Furnace



- Decisive process for absorber formation
- Product introduced in 2010
- 8 Machines already sold / FAT for 1. machine passed with very high performance values
- Up to 25 MW capacity per machine

CISARIS - Temperature Homogeneity

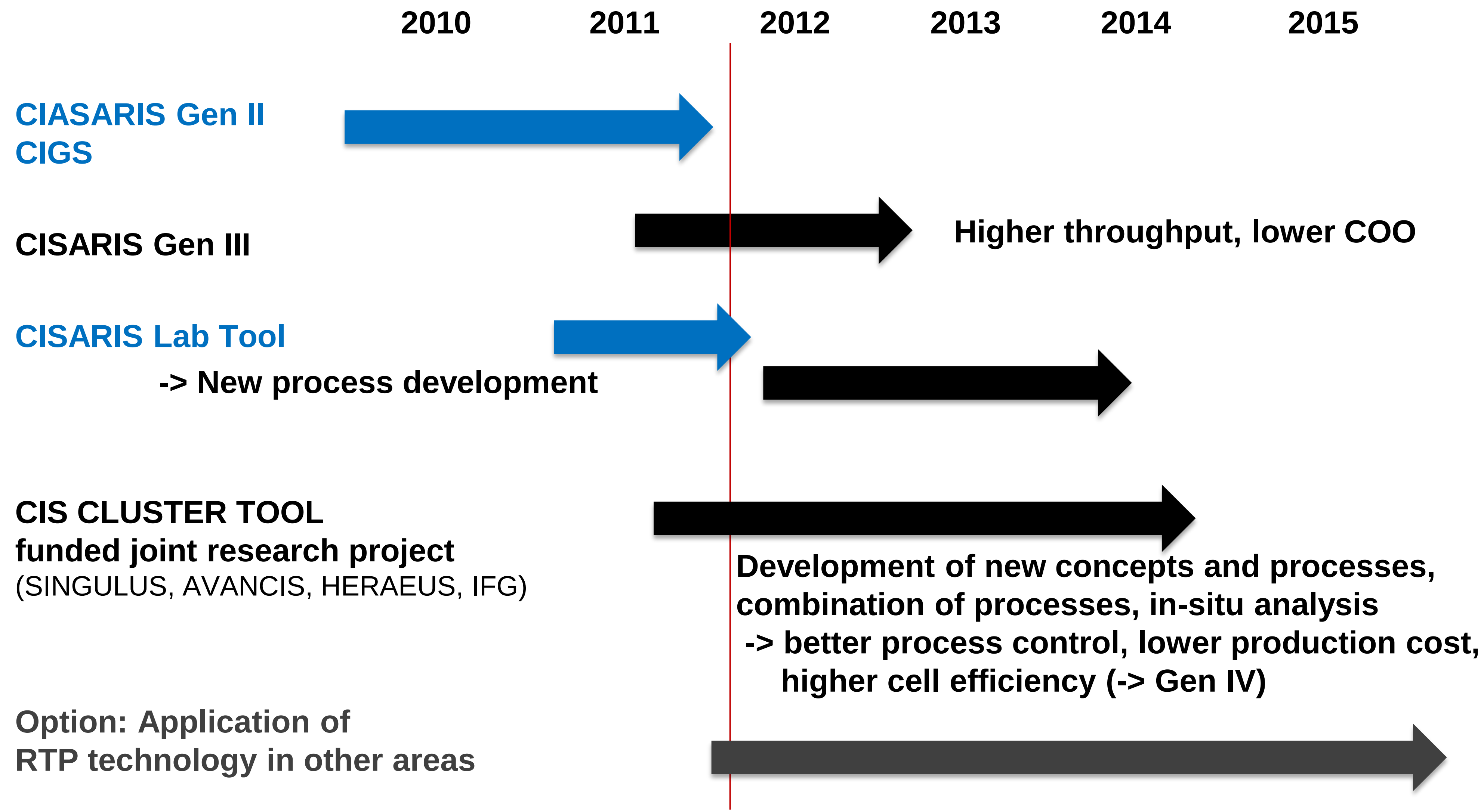
Very high temperature homogeneity and reproducibility



					F	Name	Besc...	Wert	M.	Max...	Alar...	IO-Port
V				☑	5	Zone 2.Mittelwert		495,5 °C				
V				☑	6	Zone 2.Minimum		477,4 °C				
V				☑	7	Zone 2.Maximum		506,5 °C				
V				☑	8	Zone 2.Sigma		4,7 °C				
V				☑	9	Zone 3.Mittelwert		492,8 °C				

Sigma 4,7°C

Technology Roadmap CISARIS



2010 2011 2012 2013 2014 2015

CIASARIS Gen II
CIGS

CISARIS Gen III

Higher throughput, lower COO

CISARIS Lab Tool

-> New process development

CIS CLUSTER TOOL
funded joint research project
(SINGULUS, AVANCIS, HERAEUS, IFG)

Development of new concepts and processes, combination of processes, in-situ analysis
-> better process control, lower production cost, higher cell efficiency (-> Gen IV)

Option: Application of
RTP technology in other areas

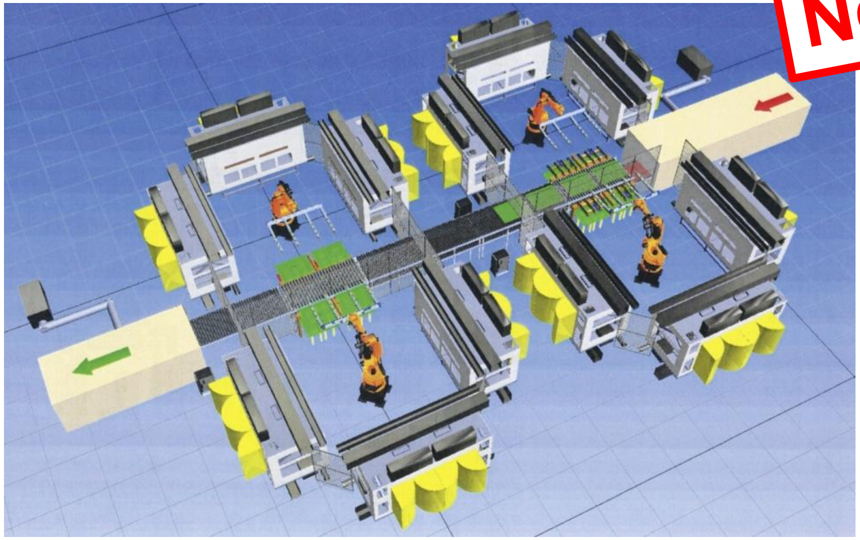
Buffer Layer - TENUIS: Best in Class

State-of-the-art production tool for Chemical Bath Deposition (CBD) buffer layers

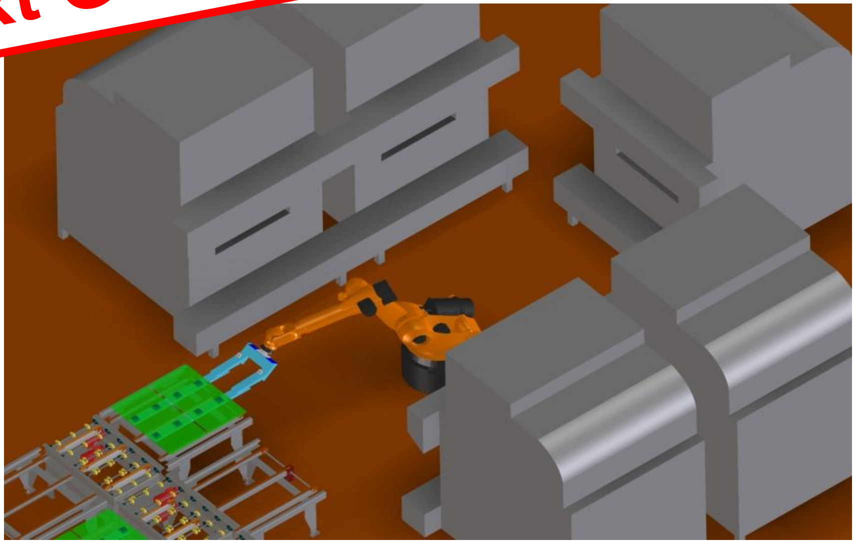
- High efficiency for all known CIS/CIGSSe absorber types
- High market penetration (> 150 process modules installed, appr.75 % market share)
- Superior to batch systems due to patented wobbling movement
  - Very low material consumption
  - Very high layer homogeneity
  - No substrate rear cleaning

Buffer Layer - TENUIS Gen II

Next Generation



*TENUIS GEN II production line

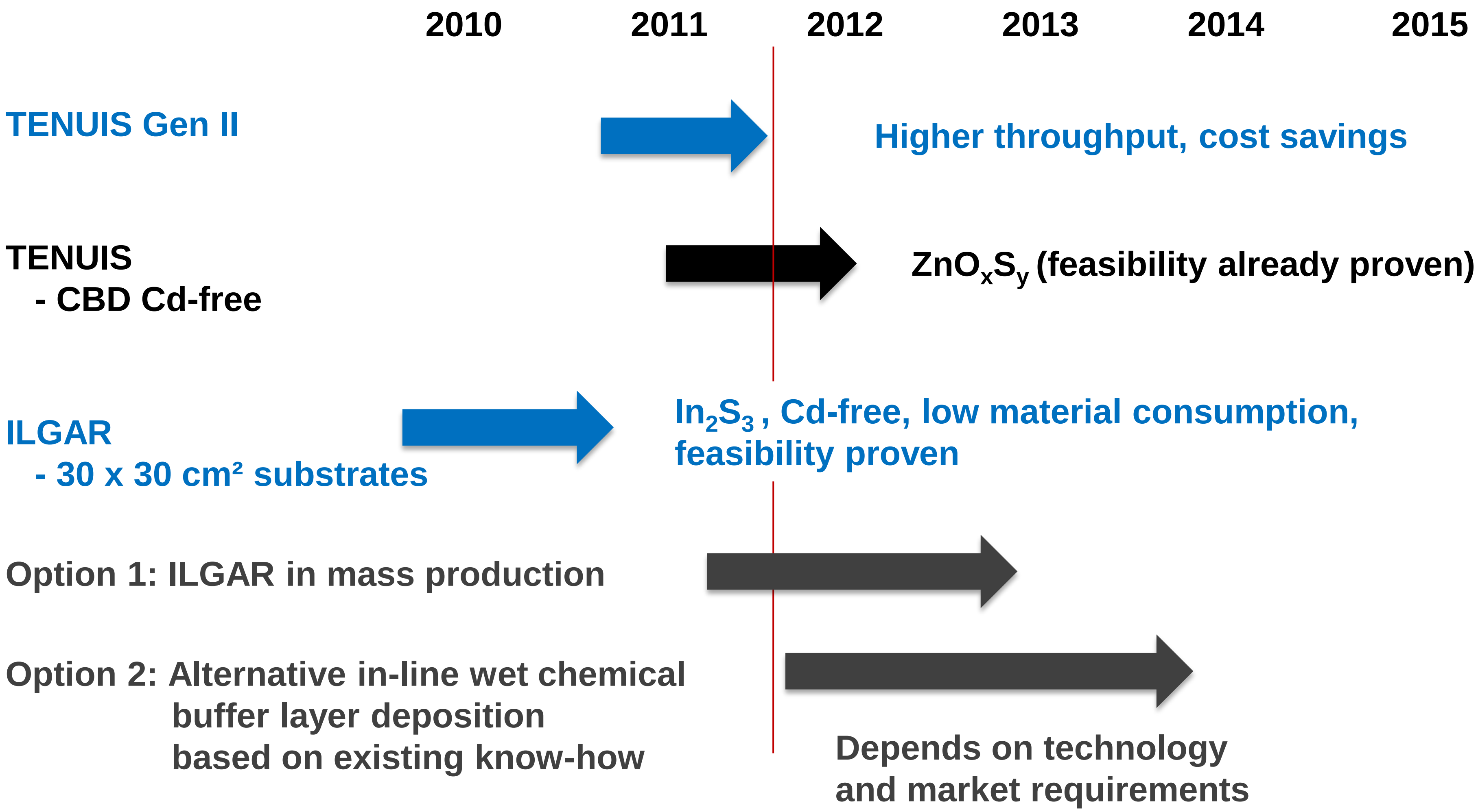


*Simultaneous process of two substrates

Improvements

- 30% cost savings in total
- Reduced footprint of up to 50%
- Reduced maintenance costs
- New processes for alternative buffer materials (ZnO_xS_y, In_2S_3)
- More precise process control allows higher throughput
- New software surface and applications for more flexibility

Technology Roadmap Buffer Layer Deposition



2010 2011 2012 2013 2014 2015

TENUIS Gen II

Higher throughput, cost savings

TENUIS
- CBD Cd-free

ZnO_xS_y (feasibility already proven)

ILGAR
- 30 x 30 cm² substrates

In_2S_3, Cd-free, low material consumption, feasibility proven

Option 1: ILGAR in mass production

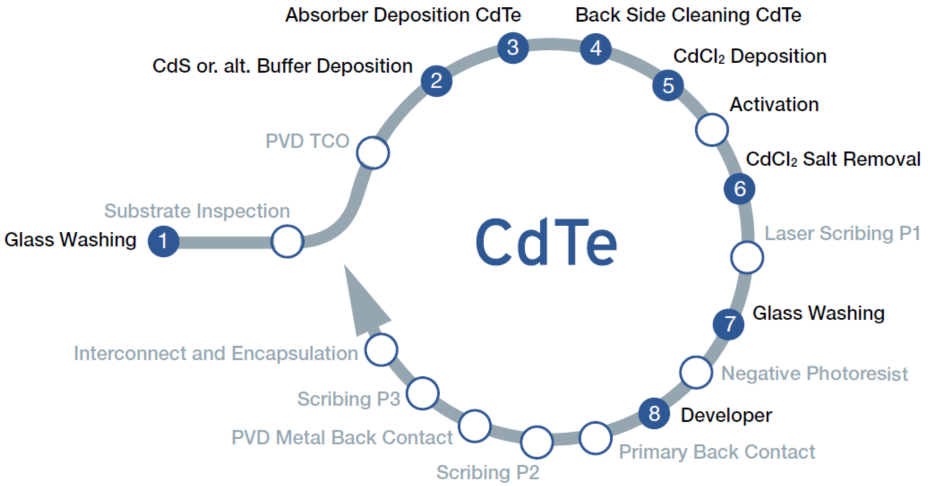
Option 2: Alternative in-line wet chemical
buffer layer deposition
based on existing know-how

Depends on technology
and market requirements

VITRUM Gen II - Etching and Cleaning (CIGS/CdTe)

- New modular design - high versatility
- Lowest cost of ownership on the market
- High availability (uptime > 98%)

- Broad field of applications in CIGS and CdTe thin film module production



1. VITRUM Clean
2. TENUIS altn. ILGAR® or IMPEDIO
3. COATER CdTe
4. VITRUM Etch
5. VITRUM Coating
6. VITRUM Clean
7. VITRUM Clean
8. VITRUM Developer

● SINGULUS
○ Cooperation Partner

VITRUM Gen II - Advanced Applications

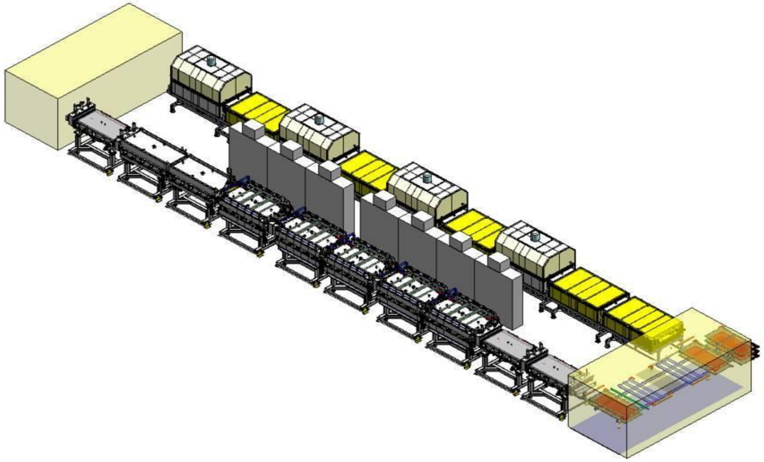
- Replacing dipping processes by simpler in-line procedures with lower material usage and higher process speed

- Unique application for rear side cleaning and edge cleaning after active layer deposition without absorber damage (only available tool in the market)

- Option for many other wet chemical processes for thin film PV

Summary Roadmap Thin Film

Keep focus on CIGS, integration of additional processes, further extension and transfer of core technologies



- Further extension of diffusion furnace knowledge
  - new generation **CISARIS**
  - application for various absorber formation processes
  - transfer to other application fields (e.g. CdTe)

- Further development of processes and hardware for buffer layer formation (Cd-free / **TENUIS** / **ILGAR** / new in-line processes)

- Further extension of the modular **VITRUM** to new processes and applications

- Combination and integration of machines and processes

- Continued cooperation with industrial partners and research institutes to further increase cell efficiency and to reduce production cost

PV Technology Roadmap - Conclusion

- SINGULUS is well positioned in the attractive, further growing solar market, offering “wet & vacuum” key technologies in the fields of c-Si and thin film photovoltaics

- Originating from these core technologies, SINGULUS designs and delivers dedicated new equipment and processes to reduce production cost and to increases cell efficiencies.

  A transfer of technologies to other cell concepts is done for promisiong applications.

  Different processes are integrated to reduce complexity and cost.

- New achievements and a clear roadmap have been demonstrated for c-Si and thin film applications.

- SINGULUS permanently keeps on developing new processes and equipment in cooperation with research institutes and industrial partners.

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